MoSys, Inc.
Form 10-K
March 14, 2014

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UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K

ý **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the Fiscal Year December 31, 2013 or

o **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

Commission file number: 000-32929

MOSYS, INC.

(Exact name of registrant as specified in its charter)

Delaware	**77-0291941**
(State or other jurisdiction of incorporation or organization)	(IRS Employer Identification Number)

3301 Olcott Street
Santa Clara, California 95054
(Address of principal executive offices)
(408) 418-7500
(Registrant's telephone number, including area code)

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	**Name of each exchange on which registered**
Common Stock, par value $0.01 per share	Global Select Market of the NASDAQ Stock Market, LLC

Securities registered pursuant to Section 12(g) of the Act:

Title of each class	Name of each exchange on which registered
Series AA Preferred Stock, par value $0.01 per share	None

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes o No ý

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes o No ý

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ý No o

Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes ý No o

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K (§ 229.405 of this chapter) is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. ý

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See definition of "large accelerated filer," "large accelerated filer" and "smaller reporting company" in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer o	Accelerated filer ý	Non-accelerated filer o (Do not check if a smaller reporting company)	Smaller reporting company o

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes o No ý

The aggregate market value of the common stock held by non-affiliates of the registrant, as of June 30, 2013 was $187,432,524 based upon the last sale price reported for such date on the Global Select Market of the NASDAQ Stock Market. For purposes of this disclosure, shares of common stock held by persons who beneficially own more than 5% of the outstanding shares of common stock and shares held by officers and directors of the Registrant have been excluded because such persons may be deemed to be affiliates. This determination is not necessarily conclusive.

As of March 1, 2014, 49,165,240 shares of the registrant's common stock, $0.01 par value per share, were outstanding.

DOCUMENTS INCORPORATED BY REFERENCE

Portions of the registrant's proxy statement to be delivered to stockholders in connection with the registrant's 2014 Annual Meeting of Stockholders to be held on or about June 3, 2014 are incorporated by reference into Part III of this Form 10-K. The registrant intends to file its proxy statement within 120 days after its fiscal year end.

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ANNUAL REPORT ON FORM 10-K
FOR THE YEAR ENDED DECEMBER 31, 2013

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Part I

This Annual Report on Form 10-K and the documents incorporated herein by reference contain forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, which include, without limitation, statements about the market for our products, technology, our strategy, competition, expected financial performance and other aspects of our business identified in this Annual Report, as well as other reports that we file from time to time with the Securities and Exchange Commission. Any statements about our business, financial results, financial condition and operations contained in this Annual Report that are not statements of historical fact may be deemed to be forward- looking statements. Without limiting the foregoing, the words "believes," "anticipates," "expects," "intends," "plans," "projects," or similar expressions are intended to identify forward-looking statements. Our actual results could differ materially from those expressed or implied by these forward-looking statements as a result of various factors, including the risk factors described in Part I., Item 1A, "Risk Factors," and elsewhere in this report. We undertake no obligation to update publicly any forward-looking statements for any reason, except as required by law, even as new information becomes available or other events occur in the future.

Item 1. Business

Overview

MoSys, Inc., together with its subsidiaries ("MoSys," the "Company," "we," "our" or "us"), is a fabless semiconductor company focused on the development and sale of integrated circuits, or ICs, for the high-speed networking, communications, storage and computing markets. Our technology delivers time-to-market, performance, power and economic benefits for system original equipment manufacturers, or OEMs. We have developed a family of ICs, called Bandwidth Engine, which combines our proprietary 1T-SRAM high-density embedded memory and high-speed 10 gigabits per second, or Gbps, and higher serial interface, or I/O, with our intelligent access technology and a highly efficient interface protocol. As the bandwidth requirements and amount of packet processing increase in high-speed networking systems, critical memory access bottlenecks can occur. Our Bandwidth Engine IC, with its combination of serial I/O, high-speed memory, and efficient, intelligent access, drastically increases memory accesses per second, removing these bottlenecks. In March 2013, we announced another IC product line under the LineSpeed product name. LineSpeed ICs are non-memory, high-speed SerDes I/O devices with gearbox and retimer functionality, which convert lanes of data received on line cards into different configurations and/or ensure signal integrity. These ICs are designed for next-generation ethernet and optical transport network applications. Historically, our primary business was the design, development, marketing, sale and support of differentiated intellectual property, or IP, including embedded memory and high-speed parallel and serial I/O used in advanced systems-on-chips, or SoCs. Currently, we are focused on developing differentiated IP-rich IC products and are dedicating substantially all of our research and development, marketing and sales budget to these IC products.

Our future success and ability to achieve and maintain profitability will be dependent on the marketing and sales of our IC products into networking, communications and other markets requiring high-bandwidth memory access. Since the beginning of 2010, we have invested an increasing amount of our research and development resources towards development of our ICs, and as of the end of 2012 had ceased our efforts to actively market our IP and establish license agreements for customers' new SoC development projects. However, we have made opportunistic sales of some of our IP. For instance, in December 2011, we sold a number of patents in an arrangement that provided $35 million

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in cash with no equity dilution to the Company and, in March 2012, we sold a portion of our SerDes technology and supporting workforce for approximately $4.3 million.

Due to the shift in our engineering and research and development focus and the decline in major consumer electronics applications utilizing customized versions of our 1T-SRAM technology, the competitiveness of, and demand for, our IP have declined since the beginning of 2011. While, we expect royalty revenue to continue to represent a significant portion of our revenues in 2014, albeit at a reduced level, we expect our revenue to transition to predominately IC product sales in 2014. To date, we have not generated significant revenue from sales of our IC products, and revenue from IP licensing and royalties represented the majority of our revenues for 2013. We are currently supporting existing design win customers and actively pursuing additional design wins for the use of our ICs in networking and communication equipment. We have established initial pricing of our IC products ordered to date, but longer-term volume prices will be subject to negotiations with our customers and may vary substantially from these initial prices.

Industry Background

The amount of data being transferred by networking, storage and computing systems is increasing rapidly, primarily driven by the growth of the Internet and demand for real-time processing of bandwidth intensive applications, such as video-on-demand, Internet protocol TV, peer-to-peer and cloud computing, web2.0 applications, 3G/4G wireless, voice-over-Internet protocol, and many others. In order to meet these demands, the network backbone, access, storage and data center infrastructure must scale in bandwidth and processing capability. In addition, system designers face the challenge of increasing the throughput of all subsystems for a variety of applications, such as video games, medical record and imaging transfers, and file sharing. These increased demands strain communication between onboard IC devices, limiting the data throughput in network switches and routers and the network backbone. To meet this demand, carrier and enterprise networks are undergoing significant changes and, most significantly, are migrating to packet-based Ethernet networks that enable higher throughput, lower cost and uniform technology across access, core and metro network infrastructure. These networks are now being designed to deliver voice, video and high-speed Internet access on one converged, efficient and flexible network. These trends require networking systems, especially the high-speed switches and routers that primarily comprise these networks, to comply with evolving market requirements and be capable of providing new services, better quality of service while supporting new protocols and standards. To support these trends, the next generations of networking systems must offer higher levels of packet forwarding rates, bandwidth density and be optimized to enable higher-density, lower power data path connectivity. This in turn necessitates new generations of packet processors and improved memory subsystems to enable system performance in support of these increased demands.

The OEM companies that produce networking and communications systems include Alcatel-Lucent, Brocade Communications Systems, Inc., Cisco Systems, Inc., Tel. LM Ericsson, Fujitsu Ltd., Hitachi Ltd., Huawei Technologies, Juniper Networks, Inc., Nokia Siemens Networks, and ZTE Corporation, as well as many other smaller suppliers. The networking and communications systems in the network backbone that must operate at higher speed and performance levels include the following types of routers, switches and other appliances: core, carrier Ethernet, edge, metro Ethernet, optical transport and service. In addition, networking and communications systems that sit on the edge of data centers, such as edge routers, aggregation switches and load-balancing and security appliances, must also operate at higher speed and performance levels. These networking and communications systems are typically built as a modular, multi-slot chassis that consists of several line cards with many network ports per line card or as a stand-alone, fixed configuration, flat frame containing multiple network line cards. These systems and their component line cards will generally need to support aggregate rates above 100 Gbps to meet the continued growth in network traffic. The type and number of semiconductors included on the line cards depend on the capacity, port type and target functionality of

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each card. Several types of semiconductors are included on each line card, including physical interface electronics, one or more packet processors and multiple memory chips. Packet processors are complex ICs developed using field programmable gate arrays, or FPGAs, application-specific integrated circuits, or ASICs, application specific standard products, or ASSPs, or network processing units, or NPUs, that perform high speed processing for functions, such as traffic shaping, metering, billing, statistics, detection and steering. Various types of memory ICs are used in order to facilitate the temporary storage and assist in the analysis and tracking of information embedded within each packet flowing through the processors. After a packet enters the line card through a physical interface, a packet or data processor helps separate the packet into smaller pieces for rapid analysis. Typically, the data is broken up into the packet header, which contains vital information on packet destination and type, such as the internet protocol address and payload, which contains the data being sent. In a basic operation, the packet header is stripped from the packet, and processed separately by the packet processing engine on the line card. The analysis of the packet header must occur at full data rates and typically requires accessing memory ICs many times. Simultaneously, the packet's payload, which may be substantially larger than the packet header, is also stored in memory ICs. Once processing is complete, the packet is re-combined to be sent from the system. Within the line card, communication between the packet processor and memory ICs occurs through either a parallel or serial interface. Combinations of physical pins on each type of chip are grouped together in a parallel or serial architecture to form a pathway, called a bus, through which information is transferred from one IC to the next.

Today, the majority of physical buses use a parallel architecture to communicate between processors and memory ICs, which means information can travel only in one direction and in one instance at a time. As processing speeds increase, in a parallel architecture the number of pins required and the speed of the bus become a limitation on system performance and capability. In a serial architecture, the number of connections is reduced substantially across fewer, higher-rate pins and data is transferred simultaneously in both directions. High speed serial bus architectures and more advanced I/O protocols must be supported by the various ICs included on the line card in order to remove the bottleneck and meet next generation bandwidth requirements.

The majority of networking systems sold and in operation today includes line cards that process data at speeds of 10 Gbps to 40 Gbps, supporting many aggregated slower ports. To accommodate the substantial and growing increase in demand for networking communications and applications, networking systems manufacturers are developing and bringing to market next-generation systems that run at aggregate speeds of 100 to 400 Gbps with plans to scale to thousands of Gbps, or Terabits, per second. Another major challenge to system designers is what we call the "memory performance barrier." Processor performance in applications such as computing and networking have continued to nearly double every 18 months, or even sooner, while the performance of memory technology has generally been able to double once every 10 years. Existing memory IC solutions based on parallel I/O architecture easily support speeds up to 40 Gbps, but are not optimal for meeting speeds of 100 Gbps and beyond due to system-level limitations for pin counts, power and performance. Traditional memory solutions currently used on line cards include both dynamic random access memory, or DRAM, and static random access memory, or SRAM, IC solutions. Line cards in networking systems use both specialized, high-performance DRAM ICs, such as reduced-latency DRAM, or RLDRAM, low-latency DRAM, or LLDRAM, and commodity DRAM, such as double data rate, or DDR ICs. In addition, networking systems use higher-performance SRAM ICs such as quad data rate, or QDR SRAM. Substantially all of these DRAM and SRAM memory ICs use parallel interfaces, which are slower than serial interfaces and will be challenged to meet the performance requirements of networking systems greater than 100 Gbps. The result is a gap between processor and memory performance. To meet the higher performance requirements being demanded by the industry, while using current components and architectural approaches, system designers must add more discrete memory ICs to the line cards and/or add more embedded memory on the packet processor. This results in higher cost and power

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consumption, the use of more space on the line cards and additional communication interference between the ICs, which in turn results in additional bandwidth limitation problems.

We have developed our Bandwidth Engine and LineSpeed family of ICs to synergistically address the need for high-speed data access and throughput currently confronting networking system designers. We expect our IC products to meet the increasing demands placed on conventional memory technology used on the line cards in high-bandwidth networking systems. We believe that our products and technology are well positioned as replacements for existing IC solutions in order to meet the needs of the next-generation networking systems that will require a large number of packet lookups and to support aggregated rates greater than 100 Gbps. However, we believe that networking and communications systems OEMs typically prefer to extend the use of traditional memory solutions and their parallel interfaces, despite performance and costs challenges and are reluctant to change their technology platforms and adopt new designs and technologies, such as serial interfaces, which are an integral part of our product solutions. Therefore, our principal selling and marketing activities to date have been focused on persuading these OEMs and key component suppliers that our solutions provide critical performance advantages, as well as on securing design wins with them. As of December 31, 2013, we had achieved approximately 20 such design wins, which we define as the point at which a customer has made a commitment to build a board against the fixed schematic for his system, and this board will utilize our ICs. However, there is no assurance that these customer designs will be shipped in volume production to their end customers.

Our Technology

Our historical business was focused on the licensing of our proprietary 1T-SRAM and SerDes I/O technologies. We leveraged our proprietary IP to design our IC products. The following discussion explains these technologies in further detail.

On-chip Functionality

A significant performance bottleneck in any network line card is the need to transfer data between discrete ICs. Many of these data-transfer operations are iterative in nature, requiring subsequent, back-to-back accesses of the memory IC by the processor IC. Our Bandwidth Engine ICs have an arithmetic logic unit, or ALU, which enables the Bandwidth Engine IC to perform mathematical operations on data. By moving certain processing functions from the processor IC to the Bandwidth Engine IC through the use of this embedded ALU, the number of I/O transactions is reduced and the processor IC is freed up to perform other networking or micro-processing functions.

High-Performance Interface

High-speed, efficient I/Os are critical building blocks to meet high data transfer rate requirements for communication between ICs on network line cards. We believe that current networking system requirements necessitate an industry transition from parallel I/O to serial I/O. As a result, semiconductor companies are increasingly turning to serial I/O architectures to achieve needed system performance. For example, high-performance ICs that are sold into wide markets, such as FPGAs and NPUs, are using serial I/Os to ensure they can match the performance of, and compete with ASICs. While SerDes I/Os provide significantly enhanced performance over parallel I/Os, SerDes I/Os have higher power consumption, which is a challenge for IC designers. Our SerDes I/Os are tuned for low-power consumption to meet our customers' stringent power consumption requirements. Using serial I/O, IC developers also are able to reduce pin count (the wired electrical pins that connect an IC to the network line card on which it is mounted) on the IC. With reducing geometries, the size of most high-performance ICs is dictated by the number of pins required, rather than the amount of logic and memory embedded in the chip. As a result, using serial I/O facilitates cost reduction and reduced

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system power consumption, while improving the performance of both the IC itself and the overall system.

We make our I/O technologies compliant with industry standards so that they can interoperate with interfaces on existing ICs. In addition, we make them programmable to support multiple data rates, which allows for greater flexibility for the system designer, while lowering their development and validation costs. Interoperability reduces development time, thereby reducing the overall time to market of our customers' ICs.

Analog Design Capabilities

We have invested in personnel needed to define, design and market high-performance analog IC products. We have built a team of experienced engineers who combine industry expertise with advanced semiconductor design expertise to meet customer requirements and develop new products to bring to market. We intend to leverage these capabilities to achieve new levels of integration, power reduction and performance, enabling our customers to achieve differentiation in their end systems.

GigaChip Interface Protocol

In addition to the physical characteristics of the serial I/O, the protocol used to transmit data is also an important element that impacts speed and performance. To address this and complement our Bandwidth Engine devices, we have developed the GigaChip Interface, or GCI, which is an open-interface transport protocol optimized for efficient chip-to-chip communications. The GCI electrical interface is compatible with the current industry standard (Common Electrical Interface, release #11, or CEI-11). GCI can enable highly efficient serial chip-to-chip communications, and its transport efficiency averages 90% for the data transfers it handles. GCI is included in our Bandwidth Engine ICs, and we are offering it to customers and prospective partners on terms intended to encourage widespread adoption.

High-Performance and High-Density Memory Architecture

The high-density of our proprietary 1T-SRAM technologies stems from the use of a single- transistor, or 1T, which is similar to DRAM, with a storage cell for each bit of information. Embedded memory utilizing our 1T-SRAM technologies is typically two to three times denser than the six-transistor storage cells used by traditional SRAM, or 6T-SRAM. Embedded memory utilizing our 1T-SRAM technologies typically provides speeds essentially equal to or greater than the speeds of traditional SRAM and DRAM, particularly for larger memory sizes. Our 1T-SRAM memory designs can sustain random access cycle times of less than three nanoseconds, significantly faster than embedded 6T-SRAM technology. Embedded memory utilizing our 1T-SRAM technologies can consume as little as one-half the active power and generate less heat than traditional SRAM when operating at the same speed. This reduces system level heat dissipation and enables reliable operation using lower cost packaging. The Bandwidth Engine uses our 1T-SRAM high-density memory technology to provide the density of DRAM and the speed of SRAM. The internal multi-bank memory array architecture used in our Bandwidth Engine ICs enables concurrent access operations. We believe that this architecture is also optimized for small algorithmic operations and data transfers, such as packet header analysis.

Carrier and Enterprise Grade Quality and Reliability

Networking systems providers focused on the carrier and enterprise market have rigid performance and reliability standards that they require their IC vendors to achieve. Our Bandwidth Engine architecture and interface are designed for data robustness and employ end-to-end error checking and correction codes. Although the Bandwidth Engine functions as more than a discrete memory device,

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the onboard memory array represents a significant portion of the total chip area. Memory-dominated devices require substantially different and more robust testing than non-memory ICs in order to achieve the quality and reliability requirements of advanced networking systems. We have considered these requirements for our target customers and market segments and have incorporated appropriate design and manufacturing performance margins into our Bandwidth Engine IC products. As a result, our first generation Bandwidth Engine ICs passed extensive reliability and life tests required for carrier and enterprise grade qualification certification as part of its release to production. To date, our second generation Bandwidth Engine ICs have substantially passed these tests, and we expect to achieve certification in the first half of 2014.

Our Strategy

Our primary business objective is to become an IP-rich fabless semiconductor company offering ICs that deliver unparalleled bandwidth performance for next generation networking systems. The key components of the expansion of our strategic plan to become an IC supplier include the following strategies:

Target Large and Growing Markets

Our initial strategy is to target the multi-billion dollar networking and telecommunications equipment market, and to date, we have secured multiple design wins with networking and telecommunications OEMs. We are engaged with both existing customers and customer prospects, where we are working to achieve design wins, and we refer to these engagements as design-wins-in-progress.

Leverage Technologies to Create New Products

Our strategy is to combine our proprietary IP and design and applications expertise to address the needs of several upcoming generations of advanced networking systems. We believe an IC combining our 1T-SRAM and serial I/O with logic, such as in an ALU, and other functions can provide a system-level solution and significantly improve overall system performance at lower cost while using less power. Another strategy is to leverage our high-speed serial I/O to create non-memory denominated ICs. To date, we have leveraged our serial I/O and analog design capabilities to bring our initial LineSpeed IC product family to market in 2013.

Expand Adoption of the GigaChip Interface Protocol

Our goal is for our GCI interface protocol to become an open industry standard that is designed into other ICs in the system, as we believe this will further enable serial communication on network line cards and encourage adoption of our Bandwidth Engine IC products. A number of IC providers have publicly announced their intention to support GCI, including the largest FPGA providers, Altera Corporation and Xilinx, Inc., with whom we work closely to support common customers. In addition, multiple networking systems companies, including actual and prospective customers, have adopted GCI.

Build Long-Term Relationships with Suppliers of Packet Processors

We believe that having long-term relationships with packet processor providers is critical to our success, as such relationships may enable us to reduce our time-to-market, provide us with a competitive advantage and expand our target markets. A key consideration of network system designers is to demonstrate interoperability between our Bandwidth Engine IC and the packet processors utilized in their systems. To obtain design wins for our Bandwidth Engine IC, we must demonstrate this interoperability, and also show that our IC works optimally with the packet processor to achieve the performance requirements. In addition, packet processor suppliers must adopt our GCI interface. To

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that end, we have been working closely with FPGA, ASIC and NPU providers, to enable interoperability between our Bandwidth Engine IC products and their high-performance products. To facilitate the acceptance of our Bandwidth Engine ICs, we have made available development and characterization kits for system designers to evaluate and develop code for next-generation networking systems. Our characterization kits are fully-functional hardware platforms that allow FPGA and ASIC providers, and their customers, to demonstrate interoperability of the Bandwidth Engine IC with the ASIC or FPGA the designers use within their networking systems.

Our Products

Bandwidth Engine

The Bandwidth Engine is a memory-dominated IC that has been designed to be a high-performance companion IC to packet processors. While the Bandwidth Engine primarily functions as a memory device with a high-performance and high-efficiency interface, it also can accelerate certain processing operations by serving as a co-processor element. Our Bandwidth Engine ICs combine: (1) our proprietary high-density, high-speed, low latency embedded memory, (2) our high-speed serial interface technology, or SerDes, (3) an open-standard interface protocol and (4) intelligent access technology. We believe an IC combining our 1T-SRAM memory and serial I/O with logic and other intelligence functions provides a system-level solution and significantly improves overall system performance at lower cost, size and power consumption. Our Bandwidth Engine ICs can provide up to and over 4.5 billion accesses per second, which is more than twice the performance of current memory-based solutions. They also can enable system designers to significantly narrow the gap between processor and memory IC performance. Customers that design Bandwidth Engine ICs onto the line cards in their networking systems will re-architect their systems at the line card level and use our product to replace traditional memory solutions. When compared with existing commercially available solutions, our Bandwidth Engine ICs may:

provide up to four times the performance;

reduce power by approximately 50%;

reduce cost by greater than 50%; and

result in a dramatic reduction in IC pin counts on the line card.

The Bandwidth Engine is a memory-dominated IC that has been designed to be a high-performance companion IC to packet processors. While the Bandwidth Engine primarily functions as a memory device with a high-performance and high-efficiency interface, it also can accelerate certain processing operations by serving as a co-processor element.

Our first generation Bandwidth Engine IC contains 576 megabytes, or MB, of memory and uses 10.3 Gbps SerDes I/O technology. Variations of this IC can have up to two interface ports, with up to eight serial receiver and eight serial transmitter lanes per port for a total of 16 lanes of 10.3 Gbps SerDes interface. These ICs include an ALU, which can perform read-modify-write operations. These ICs are tested to meet or exceed the standards for telecommunications carrier-class and enterprise-grade applications.

We brought our second generation Bandwidth Engine IC family of devices to market in 2013, and we began sampling these devices in mid-2013. These devices operate at up to 480 Gbps using sixteen 15 Gbps SerDes lanes. In addition to a speed improvement of up to 50%, the architecture will enable several family member parts with added specialized features. To date, we have announced three unique devices:

MSR620 adds burst features optimized for oversubscription buffer applications;

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MSR720 adds a write cache and memory coherency capability that allows for deterministic look ups optimized for state and que type applications; and

MSR820 delivers increased intelligence for lookup, metering and statistics applications by adding dual counters, atomic and extensive metering functions.

The devices will represent a significant improvement in speed and features, supporting aggregate line rates of up to 400 Gbps and further reduce size, pin count and power.

LineSpeed

We brought our first generation of LineSpeed products to market and began sampling in 2013. Our first LineSpeed products consist of single-chip PHY ICs, including a 100G multi-mode gearbox and a 100G Quad retimer. These devices are designed to support 10G, 40G and 100G standards for high-density line cards or modules for next generation ethernet and optical transport network applications. Built using standard CMOS technology, these devices are capable of supporting both short and long reach connections across different specifications. We do not expect to generate significant revenue from our LineSpeed ICs until 2015 or later.

IP Licensing and Distribution

Historically, we have offered our memory and I/O technologies on a worldwide basis to semiconductor companies, electronic product manufacturers, foundries, intellectual property companies and design companies through product development, technology licensing and joint marketing relationships. We licensed our IP technology to semiconductor companies who incorporated our technology into ICs that they sold to their customers. As a result of the change in our corporate strategy, since early 2012, our IP licensing activities have been limited, and we expect this to continue. We intend to avoid future licensing projects that require significant use of our engineering resources, as our engineering personnel are now focused on our IC products. However, during 2013, substantially all of our revenues were generated from licensing and royalties related to our existing licensing arrangements, as we continue to perform and deliver under outstanding license agreements and collect royalties from 1T-SRAM licensees. To date, we have substantially completed our performance obligations under our existing agreements, and we expect licensing and royalty revenues to decline in 2014.

Customers in North America accounted for 30%, 41% and 39% of our revenues for the years ended December 31, 2013, 2012 and 2011, respectively. Customers in Japan accounted for 27%, 26% and 33% of our revenues for the years ended December 31, 2013, 2012 and 2011, respectively. Customers in Taiwan accounted for 42%, 28% and 23% of our revenues for the years ended December 31, 2013, 2012 and 2011, respectively. Our remaining revenues were from customers in the rest of Asia and in Europe.

Research and Development

Our ability to compete in the future depends on successfully improving our technology to meet the market's increasing demand for higher performance and lower cost requirements. We have assembled a team of highly skilled engineers whose activities are focused on developing higher density, higher bandwidth, higher speed and lower cost next generation IC products. Development of our IC products requires the hiring of specialized chip design and product engineers, as well as significant fabrication and testing costs, including mask costs, as we bring these products to market. Our significant future research and development activities will include:

designing next generation ICs with larger memory blocks and higher-speed SerDes;

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developing versions of our Bandwidth Engine ICs with alternative features, such as lower-speed SerDes, increased intelligence or smaller memory blocks to allow us to serve a broader range of applications and systems;

developing versions of our initial LineSpeed ICs to meet customer demands, such as lower power and higher speeds;

porting our 1T-SRAM and SerDes technology to more advanced foundry process nodes to support our IC development efforts; and

developing new products that can leverage our proprietary IP portfolio and expand our market opportunity.

No development efforts are being dedicated to creating new or enhanced technology solely for use in licensing offerings.

As of December 31, 2013, we employed 85 individuals in engineering and research and development, of which 23 were employed in our design center in Hyderabad, India. For the years ended December 31, 2013, 2012 and 2011, research and development expenditures totaled approximately $23.3 million, $28.5 million and $26.2 million, respectively.

Sales and Marketing

As of December 31, 2013, we had seven sales and marketing personnel managing and supporting our efforts to secure design wins for our IC products. Our sales and marketing personnel are located in the United States, Japan and China. In addition to our direct sales team, we sell through sales representatives and distributors in the United States and Asia. We also have 8 applications engineers who support our customer engagements and work closely with our engineering team on product definition. For our products, our applications engineers must engage with the customers' system architects and designers to propose our IC and IP, e.g., GCI Interface, solutions to address their systems' challenges. In the markets we serve, the time from initial customer engagement to design win to production volume shipments can range from two to three years. Networking and communications systems can have a product life from a few years to over 10 years.

Our IP revenue has been highly concentrated, with a few customers accounting for a significant percentage of our total revenue. For the year ended December 31, 2013, Taiwan Semiconductor Manufacturing Co., Ltd., or TSMC, and Broadcom, represented 41% and 13% of total revenue, respectively. For the year ended December 31, 2012, TSMC, Broadcom and Renesas, represented 28%, 26% and 12% of total revenue, respectively. For the year ended December 31, 2011, TSMC, Renesas and Broadcom represented 23%, 17% and 12% of total revenue, respectively.

Intellectual Property

We regard our patents, copyrights, trademarks, trade secrets and similar intellectual property as critical to our success, and rely on a combination of patent, trademark, copyright, and trade secret laws to protect our proprietary rights.

As of December 31, 2013, we held approximately 71 U.S. and 16 foreign patents on various aspects of our technology, with expiration dates ranging from 2014 to 2031. We currently have approximately 51 pending patent applications in the U.S. and abroad. There can be no assurance that others will not independently develop or patent similar or competing technology or design around any patents that may be issued to us, or that we will be able to successfully enforce our patents against infringement by others.

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In December 2011, we sold 43 United States and 30 related foreign memory technology patents for $35 million in cash pursuant to a patent purchase agreement. Under the agreement, we retained a license to all of the sold patents that is unlimited with respect to our development, manufacturing and distribution of our Bandwidth Engine IC product line and any other proprietary products that we develop as long as they are not DRAM ICs. We also retained the rights necessary to renew existing 1T-SRAM licenses and to grant licenses similar in scope to identified foundries. We also retained rights to grant licenses for our second source purposes, to enable certain kinds of technology development and, to a limited extent, for certain ASIC products that incorporate one of our technology macros. However, the patent purchase agreement limits our rights to grant licenses under the sold patents outside the scope of our retained license and, in particular, limits the number of future licenses of 1T-SRAM memory technology that we can grant to developers of SoCs, which used to be the principal focus of our 1T-SRAM licensing activities.

The semiconductor industry is characterized by frequent litigation regarding patent and other intellectual property rights. Our licensees or we might, from time to time, receive notice of claims that we have infringed patents or other intellectual property rights owned by others. Our successful protection of our patents and other intellectual property rights and our ability to make, use, import, offer to sell, and sell products free from the intellectual property rights of others are subject to a number of factors, particularly those described in Part I, Item 1A, "Risk Factors."

Competition

The markets for our products are highly competitive. We believe that the principal competitive factors are:

- processing speed and performance;
- density and cost;
- power consumption;
- reliability;
- interface requirements;
- ease with which technology can be customized for and incorporated into customers' products; and
- level of technical support provided.

We believe that we can compete favorably with respect to each of these criteria. Our proprietary 1T-SRAM embedded memory and high-speed serial I/O IP provides our Bandwidth Engine ICs with a competitive advantage over alternative devices. Alternative solutions are either DRAM or SRAM-based and can support either the memory size or speed requirements of high-performance networking systems, but generally not both. DRAM solutions provide a significant amount of memory at competitive cost, but DRAM solutions do not have the required fast access and cycle times to enable high-performance. The DRAM solutions currently used in networking systems include RLDRAM from Micron Technology, Inc., or Micron, and Integrated Silicon Solutions, Inc., LLDRAM from Renesas and DDR from Samsung Electronics Co., Ltd., Micron and others. In addition, Micron has announced a hybrid memory cube DRAM product, which consists of multiple DRAMs connected with a serial interface. SRAM solutions can meet high-speed performance requirements, but often lack adequate memory size. The SRAM solutions currently used in networking systems primarily include QDR or similar SRAM products from Cypress Semiconductor Corporation and GSI Technology, Inc. The majority of the currently available SRAM and DRAM solutions use a parallel, rather than a serial I/O. To offset these drawbacks, system designers generally use more discrete memory ICs, resulting in higher power consumption and greater utilization of space on the line card. Our competitors include

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established semiconductor companies with significantly longer operating histories, greater name recognition and reputation, large customer bases, dedicated manufacturing facilities and greater financial, technical, sales and marketing resources. This may allow them to respond more quickly than us to new or emerging technologies or changes in customer requirements. Many of our competitors also have significant influence in the semiconductor industry. They may be able to introduce new technologies or devote greater resources to the development, marketing and sales of their products than we can. Furthermore, in the event of a manufacturing capacity shortage, these competitors may be able to manufacture products when we are unable to do so.

Our Bandwidth Engine ICs compete with embedded memory solutions, stand-alone memory ICs, including both DRAM and SRAM ICs, and ASICs designed by customers in-house to meet their system requirements. Our prospective customers may be unwilling to adopt and design-in our ICs due to the uncertainties and risks surrounding designing a new IC into their systems and relying on a supplier that has almost no history of manufacturing such ICs. In addition, Bandwidth Engine ICs require the customer and its other IC suppliers to implement our new chip-to-chip communication protocol, GCI. These parties may be unwilling to do this if they believe it could adversely impact their own future product developments or competitive advantages, or if they believe it might complicate their development process or increase the cost of their products. In order to remain competitive, we believe we must provide unparalleled memory IC solutions with the highest bandwidth capability for our target markets, which solutions are engineered and built for high-reliability carrier class and enterprise applications.

Our LineSpeed ICs compete with solutions offered by Applied Micro Circuits Corporation, Avago Technologies, Broadcom, Inphi Corporation, Semtech Corp., as well as other smaller analog signal processing companies. We may also compete with ASICs designed by customers in-house to meet their system requirements, as well as by optical module OEMs.

Manufacturing

We depend on third-party vendors to manufacture, package, assemble and production test our IC products, as we do not own or operate a semiconductor fabrication, packaging or production testing facility for boards and system assembly. By outsourcing manufacturing, we are able to avoid the high cost associated with owning and operating our own facilities, allowing us to focus our efforts on the design and marketing of our products.

Quality Assurance. We perform an ongoing review of product manufacturing and testing processes. Our IC products are subjected to extensive testing to assess whether their performance meet design specifications. Our test vendors provide us with immediate test data and the ability to generate characterization reports that are made available to our customers. We have achieved ISO 9001:2008 certification, and all of our manufacturing vendors have also achieved ISO 9001 certification.

Employees

As of December 31, 2013, we had 104 employees, consisting of 76 in research and development and engineering, 7 in sales and marketing, 9 in manufacturing operations and 12 in finance and administration. By location, we had 79 employees in the United States, 23 in our development center in India and 2 sales and marketing employees in Asia. We believe our future success depends, in part, on our ability to continue to attract and retain qualified technical and management personnel, particularly highly skilled design engineers involved in new product development, for which competition is intense. We believe that our employee relations are good.

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Available Information

We were founded in 1991 and reincorporated in Delaware in September 2000. Our website address is www.mosys.com. The information in our website is not incorporated by reference into this report. Through a link on the Investor section of our website, we make available our annual reports on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K, and any amendments to those reports filed or furnished pursuant to Section 13(a) or 15(d) of the Securities Exchange Act of 1934 as soon as reasonably practicable after they are filed with, or furnished to, the Securities and Exchange Commission, or SEC. You can also read and obtain copies of any materials we file with the SEC, at the SEC's Public Reference Room at 450 Fifth Street, NW, Washington, DC 20549. You can obtain additional information about the operation of the Public Reference Room by calling the SEC at 1.800.SEC.0330. In addition, the SEC maintains a website (www.sec.gov) that contains reports, proxy and information statements, and other information regarding issuers that file electronically with the SEC, including us.

Executive Officers

The names of our executive officers and certain information about them are set forth below:

Name	Age	Position(s) with the Company
Leonard Perham	70	President and Chief Executive Officer
James W. Sullivan	45	Vice President of Finance and Chief Financial Officer
Thomas Riordan	57	Chief Operating Officer and Executive Vice President
John Monson	51	Vice President of Marketing and Sales

Leonard Perham, Mr. Perham was appointed President and Chief Executive Officer in November 2007. Mr. Perham was one of the original investors in MoSys and served on our Board of Directors from 1991 to 1997. In 2000, Mr. Perham retired from Integrated Device Technology, Inc., or IDT, where he served as Chief Executive Officer from 1991 and President and board member from 1986. From March 2000 to February 2012, Mr. Perham served as a member of or chairman of the board of directors of NetLogic Microsystems, a fabless semiconductor company. Mr. Perham also has been a venture partner with AsiaTech Management, a venture capital firm. Prior to joining IDT, Mr. Perham was President and CEO of Optical Information Systems, Inc., a division of Exxon Enterprises. He was also a member of the founding team at Zilog, Inc. and held management positions at Advanced Micro Devices and Western Digital. Mr. Perham received a Bachelor of Science degree in Electrical Engineering from Northeastern University.

James W. Sullivan, Mr. Sullivan became our Vice President of Finance and Chief Financial Officer in January 2008. From July 2006 until January 2008, Mr. Sullivan served as Vice President of Finance and Chief Financial Officer at Apptera, Inc., a venture-backed company providing software for mobile advertising, search and commerce. From July 2002 until June 2006, Mr. Sullivan was the Chief Financial Officer at 8x8, Inc., a provider of voice over internet protocol communication services. Mr. Sullivan's prior experience includes various positions at 8x8, Inc. and PricewaterhouseCoopers LLP. He received a Bachelor of Science degree in Accounting from New York University and is a Certified Public Accountant.

Thomas Riordan, Mr. Riordan became our Chief Operating Officer and Executive Vice President in May 2011. Prior to joining the Company, Mr. Riordan was President and Chief Executive Officer of Exclara, a fabless semiconductor supplier of ICs for solid-state lighting from 2006 until 2010. From 2000 to 2004, Mr. Riordan served as Vice President of PMC-Sierra's microprocessor division. Mr. Riordan joined PMC-Sierra in August 2000 when it purchased Quantum Effects Devices, which he had co-founded and served as President and Chief Executive Officer. Mr. Riordan serves on the board of directors of Mellanox Technologies. Mr. Riordan holds Bachelor of Science and Master of Science

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degrees in Electrical Engineering as well as a Bachelor of Arts degree in Government from the University of Central Florida and has done post-graduate work in Electrical Engineering at Stanford University.

John Monson, Mr. Monson became our Vice President of Marketing in February 2012. In early 2014, he assumed, on a permanent basis, additional responsibilities for our sales and business development activities and became our Vice President of Marketing and Sales. Prior to joining the Company, Mr. Monson was Vice President of Marketing for Mellanox Technologies, a supplier of interconnect solutions and services, from 2009 to 2012. From 2007 to 2008, Mr. Monson was Vice President of the EDC/PhyOptik business line at Inphi Corporation. He joined Inphi Corporation through business unit acquisition of Scintera Networks, where he was Vice President of Sales and Marketing from 2005 to 2007. Previously, he held various management positions at PMC-Sierra, Inc., Lucent Technologies and AT&T Microelectronics. Mr. Monson received a Bachelor of Science degree in Electrical Engineering from the University of Minnesota.

Item 1A. Risk Factors

If any of the following risks actually occur, our business, results of operations and financial condition could suffer significantly.

We have a history of losses and are uncertain as to our future profitability.

We recorded an operating loss of $25.6 million, excluding the one-time gain on sale of assets of $0.6 million, for the year ended December 31, 2013 and ended the period with an accumulated deficit of $117.8 million. We recorded an operating loss of $31.0 million, excluding the one-time gain on sale of assets of $3.3 million, for the year ended December 31, 2012. We recorded an operating loss of $24.3 million, excluding the one-time gain on sale of patents of $35.6 million, for the year ended December 31, 2011. We expect to continue to incur operating losses for the foreseeable future as we secure customers for and invest in the commercialization of our IC products. Due to the strong commitment of our resources to research and development and expansion of our offerings to customers, we will need to increase revenues substantially beyond levels that we have attained in the past in order to generate sustainable operating profit. Given our history of fluctuating revenues and operating losses, the expected reduction in royalty and licensing revenues and challenges we face in securing customers for our IC products, we cannot be certain that we will be able to achieve profitability on either a quarterly or annual basis in the future.

Our success depends upon the networking and communications systems markets' acceptance of our ICs.

The future prospects of our business depend on the adoption and acceptance by our target markets, networking and communications equipment, of our Bandwidth Engine and LineSpeed ICs. In 2011, we began focusing our engineering, marketing and sales efforts on our IC products and de-emphasizing our technology licensing activities, which historically have been our primary revenue source. Our primary focus is on obtaining design wins, or winning competitive bids, in which customers select our IC products to design into their systems. Our prospective customers may be unwilling to adopt and design-in our ICs due to the uncertainties and risks surrounding designing a new IC into their systems and relying on a supplier that has almost no history of manufacturing such ICs. In addition, our Bandwidth Engine IC products require our customers and their other IC suppliers to implement our new and proprietary chip-to-chip communication protocol, GCI, which they may be unwilling to do. We have determined and negotiated prices with a few customers for our ICs and have gained only limited experience with the cost of making and selling these products. Thus, currently we do not know whether we will be able to profitably make and sell these products. We are investing significant resources to develop our next generation IC products, but may not introduce these new products successfully or obtain significant revenue from them.

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An important part of our strategy to gain market acceptance is to penetrate new markets by targeting market leaders to accept our IC solutions. This strategy is designed to encourage other participants in those markets to follow these leaders in adopting our solutions. If a high-profile industry participant adopts our ICs for one or more of its products but fails to achieve success with those products, or is unable to successfully implement our ICs, other industry participants' perception of our solutions could be harmed. Any such event could reduce the amount of future sales of our IC products.

We utilize a limited number of suppliers to manufacture our ICs, and, if any of these suppliers fail to support future versions of our technology, it will be difficult for us to develop and introduce new products and our business may not grow.

We are a fabless semiconductor company and use a limited number of suppliers to manufacture our ICs, and certain of these suppliers, such as our foundry, TSMC, are sole sources. We are dependent upon supply from TSMC and other suppliers to produce our ICs. Furthermore, we are dependent on TSMC to support the production of wafers for future versions of our ICs, and such production may require changes to TSMC's existing process technology. If TSMC elects to not alter their process technology to support future versions of our ICs, we would need to identify a new foundry. In addition, to date, TSMC has not provided us with a product roadmap for the 1T-SRAM technology at process nodes below 40 nanometer. If TSMC does not support our 1T-SRAM at process nodes below 40 nanometer, we would need to eventually identify a new foundry and/or no longer use our 1T-SRAM technology. Even if TSMC alters its production processes to produce wafers for future versions of our ICs, we may experience lower than anticipated manufacturing yields and device reliability problems due to the introduction of changes in production processes. Our inability to obtain supply for our existing and future IC products or to obtain the support of third party foundries for the development and manufacture of our products at smaller process geometries could materially and adversely affect our ability to achieve our strategic product development objectives and limit our prospects for future growth.

In addition, we do not have long-term supply contracts with TSMC or any of our other manufacturing suppliers, and, therefore, such suppliers are not obligated to manufacture products for us or meet our supply requirements. In addition, such suppliers are under no obligation to meet our future design specifications, except as may be provided in a particular purchase order. If we are unable to obtain an adequate supply of our current or future products from our suppliers or find alternative sources in a timely manner, we will be unable to fulfill our customer orders and our operating results will be harmed.

Because the manufacturing of integrated circuits is extremely complex, the process of qualifying a new foundry and/or other suppliers is a lengthy process and there can be no assurance that we will be able to find and qualify replacement suppliers without materially adversely affecting our business, financial condition, results of operations and prospects for future growth.

We may not achieve the anticipated benefits of becoming a fabless semiconductor company by developing and bringing to market the Bandwidth Engine and LineSpeed IC product lines.

In 2010, we expanded our business model to become a fabless semiconductor company through the development of a product line of memory ICs called the Bandwidth Engine. In March 2013, we announced a product line of SerDes ICs called LineSpeed. Our goal is to increase our total available market by creating high-performance ICs for networking and communications systems, using our proprietary technology and design expertise. This development effort has required that we add headcount and design resources, such as expensive software tools, which has increased our losses from and cash used in operations. We may not be successful in our development efforts to bring our ICs to

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market successfully nor be successful in selling ICs due to various risks and uncertainties, including, but not limited to:

- customer acceptance;
- adoption of the GCI protocol;
- difficulties and delays in our development, production, testing and marketing activities;
- the anticipated costs and technological risks of developing and bringing ICs to market;
- the willingness of our manufacturing partners to assist successfully with fabrication;
- the availability of quantities of ICs supplied by our manufacturing partners at a competitive cost;
- our ability to generate the desired gross margin percentages and return on our product development investment;
- competition from established IC suppliers;
- the adequacy of our intellectual property protection for our proprietary IC designs and technologies;
- the vigor and growth of markets served by our current and prospective customers; and
- our lack of recent experience as a fabless semiconductor company making and selling proprietary ICs.

If we experience significant delays in bringing our IC products to market or if customer adoption of our products is delayed, we may need to raise additional capital to support the product development efforts and fund our working capital needs.

Our main objective is the development and sale of our products to networking and communications systems providers and their subsystem and component vendors, and, if demand for these products does not grow, we may not achieve revenue growth and our strategic objectives.

We market and sell our ICs to networking and communications systems providers and their subsystem and component vendors. We believe our future business and financial success depends on market acceptance and increasing sales of these products. In order to meet our growth and strategic objectives, networking infrastructure OEMs must incorporate our products into their systems, and the demand for their systems must grow as well. We cannot provide assurance that sales of products will increase substantially in the future or that the demand for our customers' systems will increase. Our future revenues from these products may not increase in accordance with our growth and strategic objectives if instead our OEM customers modify their product designs, select products sold by our competitors or develop their own proprietary ICs. Thus, the future success of this part of our business depends in large part on factors outside our control, and sales of our products may not meet our revenue growth and strategic objectives.

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Our ICs have a lengthy sales cycle, which makes it difficult to predict success in this market and the timing of future revenue.

Our ICs have a lengthy sales cycle, ranging from six to 24 months from the date of our initial proposal to a prospective customer until the date on which the customer confirms that it has designed our product into its system. As lengthy, or an even lengthier period, could ensue before we would know the volume of products that such customer will, or is likely to, order. A number of factors can contribute to the length of the sales cycle, including technical evaluations of our products by the customers, the design process required to integrate our products into the customers' products and the timing of the customers' new product announcements. In anticipation of product orders, we may incur substantial costs before the sales cycle is complete and before we receive any customer payments. As a result, in the event that a sale is not completed or is cancelled or delayed, we may have incurred substantial expenses, making it more difficult for us to become profitable or otherwise negatively impacting our financial results. Furthermore, because of this lengthy sales cycle, the recording of revenue from our selling efforts may be substantially delayed, our ability to forecast our future revenue may be more limited and our revenue may fluctuate significantly from quarter to quarter. We cannot provide any assurances that our efforts to build a strong and profitable business based on the sale of ICs will succeed. If these efforts are not successful, in light of the substantial resources that we have invested, our future operating results and cash flows could be materially and adversely affected.

We expect our licensing and royalty revenues to decrease compared with our historical results, and there is no guarantee revenues from our IC products will replace these lost revenues in the near future.

In 2011, we began to place greater emphasis on our IC business and re-deploy engineering, marketing and sales resources from IP to IC activities. We are no longer actively pursuing new license arrangements, and, as a result, our license and royalty revenues in 2013 declined when compared with prior years. We do not expect to generate sufficient revenues from our IC products to approximate the level of our historical IP revenues and allow us to achieve profitability in 2014. As a result, our operating results, cash flows and financial condition for 2014 are likely to be adversely affected.

The semiconductor industry is cyclical in nature and subject to periodic downturns, which can negatively affect our revenue.

The semiconductor industry is cyclical and has experienced pronounced downturns for sustained periods of up to several years. To respond to any downturn, many semiconductor manufacturers and their customers will slow their research and development activities, cancel or delay new product developments, reduce their workforces and inventories and take a cautious approach to acquiring new equipment and technologies. As a result, our business has been in the past and could be adversely affected in the future by an industry downturn, which could negatively impact our future revenue and profitability. Also, the cyclical nature of the semiconductor industry may cause our operating results to fluctuate significantly from year-to-year, which may tend to increase the volatility of the price of our common stock.

Royalties generated from the licensing of our memory technologies are currently a key component of revenues, and, if we fail to realize expected royalties, our operating results will suffer.

Royalties generated from the licensing of our memory technologies are currently a key component of revenues, and we expect this to continue through at least 2014. Royalty payments owed to us are calculated based on factors such as our licensees' selling prices, wafer production and other variables as provided in each license agreement. The amount of royalties we will receive depends on our licensees' business success, production volumes and other factors beyond our control. This exposes our business model to risks that we cannot minimize directly and may result in significant fluctuations in our royalty revenue and operating results from quarter-to-quarter. We do not expect to enter into any new memory

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technology licensing activities, therefore the number of royalty-bearing agreements will not increase and contribute to our royalty stream. In addition, the production volumes of the current royalty-bearing products shipped by our licensees are expected to decrease; therefore we do not expect our royalty revenue to grow in future periods. Historically, royalties have generated a 100% gross margin, and any decrease in royalties adversely affects our gross margin, operating results and cash flows.

Our revenue has been highly concentrated among a small number of licensees and customers, and our results of operations could be harmed if we lose a key revenue source and fail to replace it.

Our overall revenue has been highly concentrated, with a few customers accounting for a significant percentage of our total revenue. For the year ended December 31, 2013, our two largest customers represented 41%, and 13% of total revenue, respectively. For the year ended December 31, 2012, our three largest customers represented 28%, 26% and 12% of total revenue, respectively. For the year ended December 31, 2011, our three largest